AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application. Please amend claims 1 and 14 as follows:

LISTING OF CLAIMS:

1. (Currently Amended) A timing information generating apparatus for generating timing information on a non-completed functional block whose [[design]] timing verification has not yet been completed, said timing information generating apparatus comprising:

an input/output information identifying unit for identifying intra-block input stage sequential circuits and intra-block output stage sequential circuits by comparing logical connection information with a library in which cells used for designing the non-completed functional block are registered, said intra-block input stage sequential circuits being placed in the non-completed functional block and contributing to information exchange with extra-block input stage sequential circuits outside said non-completed functional block through input pins, said intra-block output stage sequential circuits being placed in the non-completed functional block and contributing to information exchange with extra-block output stage sequential circuits outside said non-completed functional block through output pins, and the logical connection information describing connection relationships between circuit components constituting the non-completed functional block, between the circuit components and the input pins and between the circuit components and the output pins;

a delay time calculating unit for calculating first delay times from the input pins to the intra-block input stage sequential circuits in accordance with timing constraint information describing timing constraint on said non-completed functional block, and second delay times from said intra-block output stage sequential circuits to said output pins; and

a timing information output unit for outputting timing information including the first delay times and the second delay times.

2. (Original) The timing information generating apparatus according to claim 1, wherein said delay time calculating unit sets the first delay times and the second delay times such that all the input pins and output pins satisfy conditions described in the timing constraint information.

3. (Original) The timing information generating apparatus according to claim 1, wherein said delay time calculating unit sets the first delay times and the second delay times such that the input pins and output pins satisfy conditions described in the timing constraint information with leaving a same spare time uniformly for all the input pins and output pins.

4. (Original) The timing information generating apparatus according to claim 1, wherein said delay time calculating unit sets the first delay times and the second delay times such that the input pins and output pins satisfy conditions described in the timing constraint information with leaving different spare times for the individual input pins and output pins.

5. (Original) The timing information generating apparatus according to claim 1, wherein said delay time calculating unit sets the first delay times and the second delay times such that the input pins and output pins dissatisfy conditions described in the timing constraint information with leaving a same shortage of time uniformly for all the input pins and output pins.

6. (Original) The timing information generating apparatus according to claim 1, wherein said delay time calculating unit sets the first delay times and the second delay times such that the input pins and output pins dissatisfy conditions described in the timing constraint information with leaving different shortages of time for the individual input pins and output pins.

7. (Original) The timing information generating apparatus according to claim 1, further comprising a driving cell specifying unit for specifying at least one appropriate cell registered in said library as the cells for driving the output pins.

8. (Original) The timing information generating apparatus according to claim 7, wherein said driving cell specifying unit specifies a same cell for all the output pins uniformly as the cells for driving the output pins.

9. (Original) The timing information generating apparatus according to claim 7, wherein said driving cell specifying unit specifies appropriate cells for the individual output pins as the cells for driving the output pins.

10. (Original) The timing information generating apparatus according to claim 7, further comprising a load capacitance specifying unit for specifying at least one appropriate capacitance as intra-functional block load capacitances of the input pins and output pins.

11. (Original) The timing information generating apparatus according to claim 10, wherein said load capacitance specifying unit specifies a same capacitance uniformly for all the input pins and output pins as the intra-functional block load capacitances of the input pins and output pins.

12. (Original) The timing information generating apparatus according to claim 10, wherein said load capacitance specifying unit specifies appropriate capacitances for the individual input pins as the intra-functional block load capacitances of the input pins.

13. (Original) The timing information generating apparatus according to claim 10, wherein said load capacitance specifying unit specifies appropriate capacitances for the individual output pins as the intra-functional block load capacitances of the output pins.

14. (Currently Amended) A timing information generating apparatus for generating timing information on a non-completed functional block whose [[design]] timing verification has not yet been completed, said timing information generating apparatus comprising:

an input/output information identifying unit for identifying an intra-block input stage sequential circuit and an intra-block output stage sequential circuit by comparing logical connection information with a library in which cells used for designing the non-completed functional block are registered, said intra-block input stage sequential circuit being placed in the non-completed functional block and contributing to information exchange with an extra-block input stage sequential circuit outside said non-completed functional block through an input pin, said intra-block output stage sequential circuit being placed in the non-completed functional block and contributing to information exchange with an extra-block output stage sequential circuit outside said non-completed functional block through an output pin, and the logical connection information describing connection relationships between circuit components constituting the non-completed functional block, between the circuit components and the input pin and between the circuit components and the output pin;

a delay time calculating unit for calculating a first delay time from the input pin to the intra-block input stage sequential circuit in accordance with timing constraint information describing timing constraint on said non-completed functional block, and a second delay time from said intra-block output stage sequential circuit to said output pin; and

a timing information output unit for outputting timing information including the first delay time and the second delay time.